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Trade Study and Design of a TRL-4, 100 °C, 28- to 600-V Bidirectional DC-DC Converter Power Stage

by Damian Urciuoli, Robert A. Wood, and Charles W. Tipton

ARL-TR-5430 January 2011

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ERRATA SHEET

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This is an crrata sheet for ARL-TR-5430. Thc title of thc report has been corrected.
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Page	Reads	Should Read
Cover page	**Trade Study and Design of a TRL-4, 100 °C, 28- to 600-V Bidirectional DC**	**Trade Study and Design of a TRL-4, 100 °C, 28- to 600-V Bidirectional DC-DC Converter Power Stage**
Title page	**Trade Study and Design of a TRL-4, 100 °C, 28- to 600-V Bidirectional DC**	**Trade Study and Design of a TRL-4, 100 °C, 28- to 600-V Bidirectional DC-DC Converter Power Stage**
ii	Trade Study and Design of a TRL-4, 100 °C, 28- to 600-V Bidirectional DC	Trade Study and Design of a TRL-4, 100 °C, 28- to 600-V Bidirectional DC-DC Converter Power Stage

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14. ABSTRACT
We present the design of a 10-kW, bidirectional, 28- to 600-V, high temperature, technical readiness level (TRL)-4, converter power-stage in support of the Ground Combat Systems (GCS) heavy brigade combat vehicle modernization program. Five different converter topologies are compared. A current-fed, converter with a low-voltage-side (LVS) active clamp and a configurable voltage doubling high-voltage-side (HVS) are selected to meet the high voltage conversion ratio and high power density requirements. Simulations of synchronized and interleaved operation are performed to assess operation over source voltage ranges and identify component values to meet distortion spectrum specifications. Converter component selection allows for synchronous rectification to reduce system losses. Commercial-off-the-shelf (COTS) devices are specified and analyses of component volume reductions and loss savings for two silicon carbide (SiC) device replacement options are shown. A power-dense, three-dimensional model of the proposed converter package design is presented.

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Contents

List of Figures

List of Tables

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1. Introduction

Electrical power conversion system integration is a major focus of the Ground Combat Systems (GCS) heavy brigade combat vehicle modernization program and in the development of the new ground combat vehicle. The proposed architecture for these vehicle electrical systems is supported by two power distribution busses. A 600-V bus provides power to higher voltage onboard and exportable loads, and a 28-V bus sources legacy and lower voltage loads. Power generation is provided on the 600-V bus, and electrical energy is stored in a battery pack on the 28-V bus. System requirements dictate that the high and low voltage busses be linked through a bidirectional DC-DC converter to provide 600- to 28-V battery charging and enable operation of high voltage loads from battery power (28 to 600 V) independently of power generation. This bidirectional converter application requires 600-V high-voltage-side (HVS) and 28-V low-voltage-side (LVS) output power levels over a range of 10 to 30 kW. The high currents on the LVS of the converter and specifications for cooling fluid temperatures up to 100 °C and high volumetric and gravimetric power densities all provide significant converter design challenges. This report presents specifications/design goals, a converter topology trade study, and a technical readiness level (TRL)-4 test bed design for a 10-kW, 28- to 600-V, DC-DC bidirectional converter power-stage. The proposed power-stage can be operated as a standalone converter or as part of a scalable bidirectional converter. Potential benefits provided by silicon carbide (SiC) devices are also shown.

2. Design Considerations and System Requirements

The intended operating environment of the converter is the first and most important consideration of the design. With limited space aboard Army vehicle platforms, converter volume should be minimized. In most implementations, this goal also reduces converter mass. Therefore, converter topology selection is initially limited to those having comparatively low numbers of components. Galvanic isolation between the HVS and LVS of the converter is required for fault isolation, and is achieved using a transformer. Converters having higher operating temperature capability and higher efficiencies are desired to reduce vehicle cooling system overhead. Yet, high temperatures reduce the operating capabilities of most passive components such as inductors, transformers, and capacitors. Because capacitors typically have high effective thermal resistances, and most often do not interface with a heat sink, they can require significant de-ratings in multi-kilowatt converters. Converter topologies having low capacitance requirements can be more suited for compact and high temperature applications.

Converter operating parameters also affect size and weight. The size and weight of passive components are inversely related to converter switching frequency, whereas the size and losses of semiconductor switches are directly related to switching frequency. Therefore, a tradeoff must be made when selecting switching frequency for a given topology. Resonant and other soft switching converters can benefit from higher switching frequencies by having low switching losses. However, these converters can sometimes have higher conduction losses, a higher component count, or other component stresses which preclude their use in some applications. Due to component current or voltage ratings, many multi-kilowatt converters are comprised of a number of parallel stages operating at a corresponding fraction of the total converter power. The converter stages can have a common controller that provides phase delays between the switching periods of each stage, providing time interleaving, to reduce current and/or voltage ripple requirements on passive components, thereby reducing their size and weight. An added benefit of interleaved operation is that electromagnetic interference generated by the converter is usually reduced. For converters having high voltage conversion ratios (such as for this application), high turns ratio transformers can be used. However, leakage inductance generally increases with the turns ratio and voltage isolation levels, and can increase switching stresses and reduce effective voltage conversion ratios in non-resonant topologies. Planar transformers offer the advantages of low leakage inductance as a result of spatially interleaved primary and secondary windings, and also have large surface area to volume ratios that improve heat dissipation. In lower voltage implementations, power metal oxide semiconductor field effect transistors (MOSFETs) can be used for their low switching losses and ability to synchronously rectify to improve converter efficiency. This technique can also be used on the converter HVS for slight efficiency gains. These considerations and tradeoffs were simulated for different circuit topologies in this study. Design specifications for the 28- to 600-V bidirectional DC-DC converter are listed in table 1. Additional electrical power characteristics are presented in *Stryker Modernization Electric Power Characteristics for Loads*, Document # LS1080288 (*1*).

Table 1. Bidirectional 28- to 600-V DC-DC converter design specifications.

Bidirectional load power (W)	10,000
LVS steady state voltage range (*1*) (V)	25 to 29
HVS steady state voltage range (*1*) (V)	555 to 623
LVS max distortion factor (*1*)	0.035
HVS max distortion factor (*1*)	0.015
Galvanic isolation (LVS to HVS) (V)	1500
Maximum PGW inlet coolant and ambient temp (°C)	100
Coolant flow rate (lpm)	3.8 to 18.9

3. Converter Topology Comparison and Simulation Results

Five different converter topologies were compared based on design considerations. Each topology was simulated as a 5-kW power-stage (except the resonant topology) to meet system requirements with two parallel stages. In some cases, the HVS of the two stages (having reduced voltages) are connected in series. This section describes and compares the five topologies considered.

3.1 Dual Active Bridge

The full-bridge converter is a common high power isolated topology that can be designed for bidirectional operation. In its bidirectional form, the topology is referred to as a dual active bridge. It has a relatively low component count and good transformer core utilization, and can be controlled using conventional complementary switching techniques. The converter schematic is shown in boost-mode (LVS source, HVS load) in figure 1 with a full-bridge HVS stage. To reduce passive component size, a switching frequency of 50 kHz was selected. MOSFET devices were used in the converter simulation model, based on the high switching frequency (hard switched) and high LVS current. The converter was simulated in boost-mode with a transformer turns ratio of 1:20. A primary winding leakage inductance of 0.4 μH was estimated from planar transformer specifications. Simulation results showed that converter output voltage was very sensitive to leakage inductance and was approximately 270 V for a 72-Ω load, at a maximum duty cycle of 48%. This is well below the nominal output voltage of 600 V and is attributed to the high transformer leakage inductance at high switching frequency. Even with a primary leakage inductance value of 0.1 μH, which is very low even for transformers having much lower turns ratios, the load voltage increased to only about 380 V. The full-bridge HVS stage could be replaced by a half-bridge stage, which would serve as a voltage doubler in boost-mode and a half-bridge in buck-mode. This could allow for half the transformer turns ratio and reduced leakage inductance. This design modification was simulated to yield a maximum HVS voltage of only about 370 V at a 50-kHz switching frequency with a primary leakage inductance of 0.1 μH. The high transformer leakage inductance and the high switching frequency limit the performance of the dual active bridge topology in this application. Transformer winding utilization and power transferred to the load was also poor under these conditions and therefore this topology was not selected.

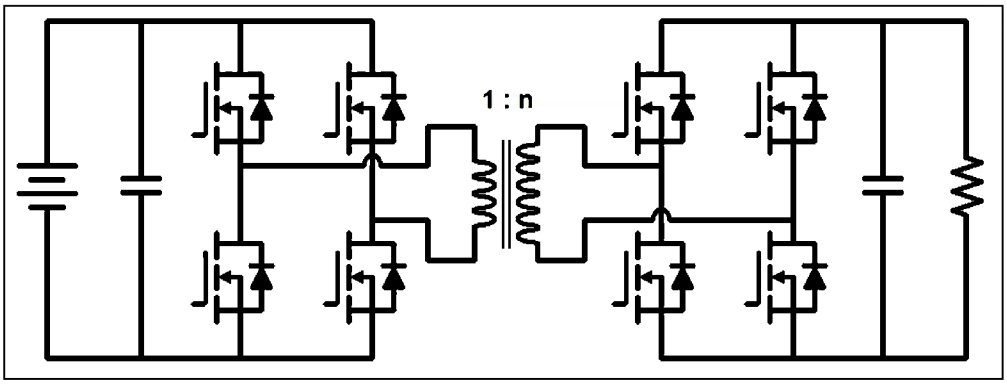

Figure 1. Dual active bridge converter schematic shown in boost-mode.

3.2 Cascaded Bidirectional and Full-bridge

The main challenge seen in the full-bridge simulations was achieving a high voltage conversion ratio in a single converter stage. To reduce the voltage conversion ratio of the full-bridge, placement of a non-isolated bidirectional DC-DC converter stage on the LVS of the full-bridge converter was considered. With the bidirectional converter stage capable of high efficiency operation at a voltage conversion of between 2 and 4, the full-bridge transformer turns ratio can be reduced to about 1:5. Having two stages allows flexibility in the voltage conversion ratios of each converter and the overall system. To further reduce the transformer turns ratio and corresponding leakage inductance, a cascaded model having a voltage doubler/half-bridge HVS stage and a full-bridge transformer turns ratio of 1:4 was simulated. The schematic of the cascaded converter is shown in figure 2.

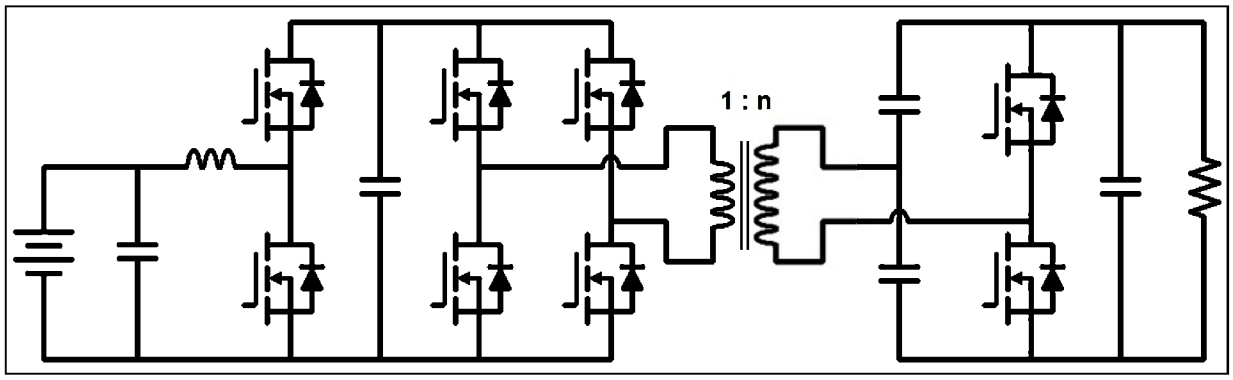

Figure 2. Cascaded bidirectional and full-bridge/half-bridge converter schematic (boost-mode).

In boost-mode, a load voltage of 600 V was simulated for 50-kHz operation, with a 72-Ω, 5-kW load. A primary leakage inductance of 0.1 μH, as specified for a custom planar transformer, was used. The bidirectional converter duty cycle was 70% and the full-bridge duty cycle was 42%. It is obvious that the topology has a higher component count than the full-bridge converter alone. Because of the large current stresses on the switch and diode of the bidirectional converter in either boost- or buck-mode, multiple parallel interleaved bidirectional converter stages would be

used. However, multiple parallel stages further increase component count and require more complex control.

An issue impacting system volume is related to the DC link capacitor placed across the HVS of the bidirectional converter (same location as the LVS of the full-bridge converter). This capacitor transforms the bidirectional converter HVS current source into a voltage source that feeds the full-bridge converter. Simulations showed the 1000-μF link capacitor to have ripple currents greater than 100 A_{RMS}. A 200-V capacitor bank satisfying these conditions and operating in a 100 °C environment would be much larger than initially anticipated and would result in a large converter volume. Therefore, other topologies were considered.

3.3 Push-Pull

The push-pull converter is a simple, transformer-isolated topology benefitting from a low component count, low conduction losses, and in most applications, ground referenced switches on the input side. All of these characteristics are advantageous on the LVS. The converter can be operated for bidirectional power flow and can have any of the secondary side configurations as the full-bridge converter. The schematic of the modeled push-pull converter in boost-mode having low side snubbers and a voltage doubler/half-bridge HVS stage is shown in figure 3.

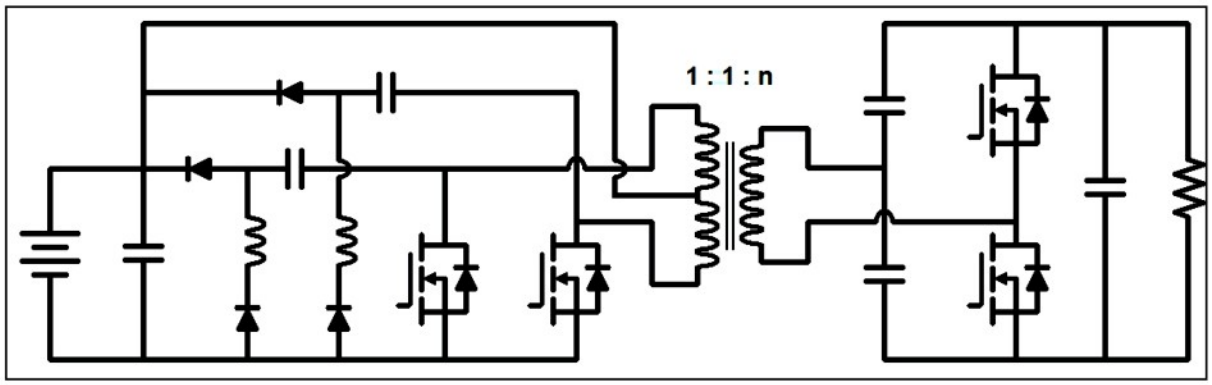

Figure 3. Push-pull converter schematic with low side snubbers (boost-mode).

Snubbers were needed on the LVS of the model to reduce high voltage stresses on the switches caused by leakage inductance of the primary winding. Unfortunately, snubbers increase the component count of this topology. The push-pull is vulnerable to switch voltage stress by not having a freewheeling path for primary current. Furthermore, the center-tapped primary winding introduces more leakage inductance than a two terminal primary. Finally, with a center tapped primary, transformer winding utilization is less than that of the full-bridge.

Simulation results of the push-pull circuit with a 1:8 transformer turns ratio (1:8 for both segments of the primary winding), resulted in an HVS voltage of 300 V for an 18-Ω, 5-kW load at a 50-kHz switching frequency. This would require the outputs of two 5-kW converter stages to be connected in series instead of the parallel connections used for the 5-kW stages of the

converters discussed above. On the LVS, the snubbers functioned in a stressful resonant mode with 2-μF capacitors having over 70 A of AC_{RMS} current, while only limiting switch voltage stress to approximately 170 V. For these realizations, the push-pull converter is not recommended for this application.

3.4 Parallel-Resonant

The parallel-resonant converter is based on the full-bridge topology with the addition of a resonant tank network. Resonant circuit operation reduces switching losses, and therefore enables higher switching frequencies. A schematic of the parallel resonant converter is shown in figure 4 with the inductor and capacitor tank network connected to the primary winding of the transformer. Because the parallel resonant topology is generally only intended for efficient unidirectional operation, a single converter stage load power of 10 kW would be required and an additional converter stage providing power flow in the opposite direction (not shown) would allow the two stages together to meet the 10-kW bidirectional goal. A unidirectional design also reduces redundancy and could have a more dramatic impact on system functionality in the event of a partial converter failure, than an inherently bidirectional topology. This converter was simulated at a switching frequency of 100 kHz. The transformer primary leakage inductance was set at 0.4 μH for a transformer turns ratio of 1:20. Inductor and capacitor values were initially selected as 0.9 μH and 3 μF, respectively, for a resonant frequency of approximately 100 kHz based on equation 1, to obtain zero current switching (ZCS) transitions with a duty cycle of 48%. In principle, the resonant frequency should be designed to be above the switching frequency; however, transformer leakage inductance also affects resonance.

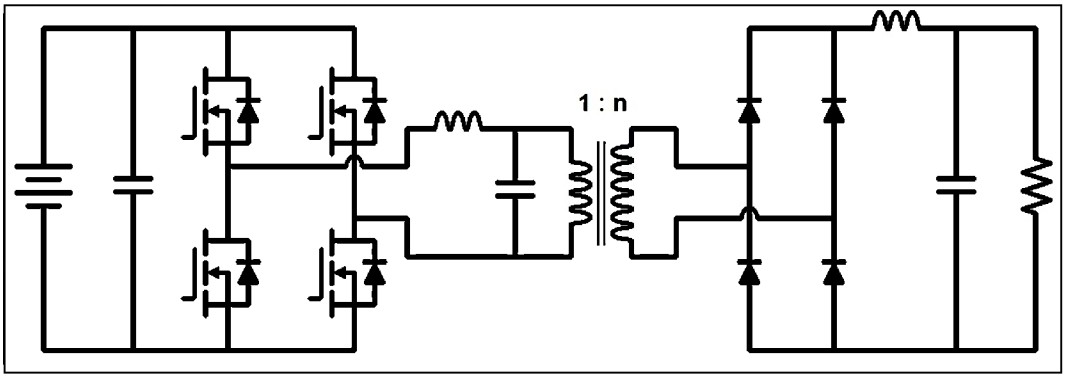

Figure 4. Parallel resonant converter schematic shown with output filter inductor.

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

During simulations, the resonant capacitor value was adjusted higher and the resonant inductor value was adjusted lower to provide more load current while preserving the ZCS condition. Unfortunately, as the capacitor value is increased, capacitor current also increases. For a light

converter load of 150 Ω at 600 V (2.4 kW), a 6-μF resonant capacitor having a current of 260 A_{RMS} was used in the simulation model. This load condition is only about one quarter of the required single-stage load of 10 kW. The resonant capacitor required to satisfy this operating condition, would have a large volume, especially for a 100 °C environment. Finally, the ZCS operating condition is generally unable to be maintained over a large load range, and thus the efficiency benefits of the topology are reduced. Considering these issues, this topology was discounted from consideration.

3.5 Bidirectional, Current-fed, Voltage Doubling (BCVD) with Active Clamp

An isolated converter topology, similar to the dual active bridge, was identified that has high voltage conversion ratio capability using a relatively low transformer turns ratio. This topology is referred to as a high step-up active-clamp converter with input-current doubler and output-voltage doubler (*2*). It was designed for unidirectional low voltage fuel cell power systems, but is capable of bidirectional power flow. The converter schematic is shown in boost-mode in figure 5 with the Greinacher voltage doubler replaced with a half wave voltage doubler on the HVS. This change was made to simplify the control of the HVS stage for bidirectional power conversion and to avoid resonant capacitor operation. The two lower switches and inductors of the LVS function as the current doubler, while the upper switches and clamp capacitor on the LVS function as an active voltage clamp to reduce voltage stress on the lower switches. On the LVS in boost-mode, each upper-switch anti-parallel diode clamps the voltage across the corresponding lower switch induced by the transformer leakage inductance at a lower-switch turn-off transition. After a short dead-time interval, the upper switch is turned on while its anti-parallel diode is still conducting to allow the energy in the clamp to be delivered to the transformer. However, if the upper switch is left on for the full complementary interval of the lower switch (excluding dead-time), the clamp energy will continue to oscillate between the transformer leakage inductance and the clamp capacitance at a resonant frequency determined by the leakage inductance and the clamp capacitance. These oscillations cause unnecessary losses in the components and can result in suboptimal energy transfer to the load. Therefore, the upper switches are turned on for a very short interval to allow energy to be transferred from the clamp to the transformer without reversal. This causes the upper switches of the LVS to operate at significantly lower duty cycles and lower root mean square (RMS) currents than the lower switches. In buck-mode, the active clamp is not used, and therefore no current is conducted by the upper switches. Synchronous rectification can be used in buck-mode to reduce conduction losses of the lower diodes on the LVS.

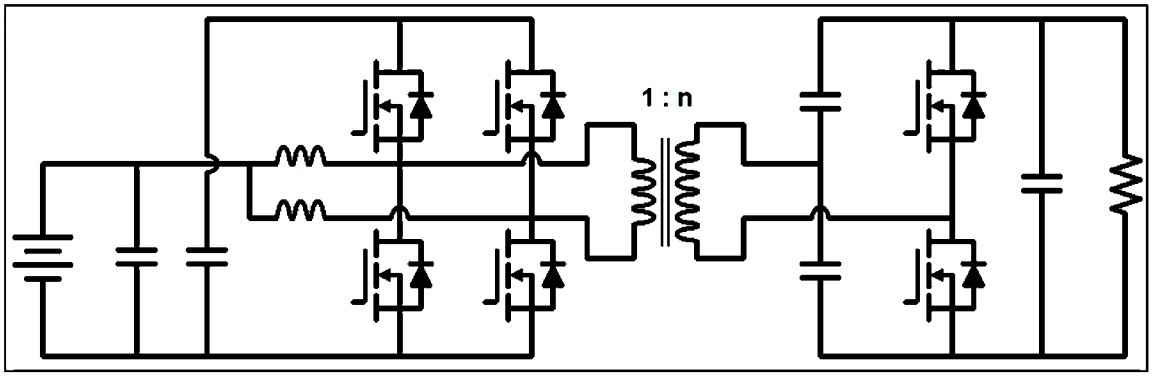

Figure 5. BCVD converter schematic with half wave voltage doubler (boost-mode).

The BCVD converter was modeled with a 1-μF clamp capacitor; 10-μH inductors; a transformer turns ratio (primary to secondary) of 1:4, with a primary winding leakage inductance of 0.1 μH and voltage doubler capacitors of 1.5 μF; a 50-kHz switching frequency; and a 72-Ω load (5 kW at 600 V). Table 2 shows RMS current values for selected converter components from a single-stage, 5-kW, boost-mode simulation. The inductors have significant RMS current, but can be designed using planar cores and windings to match the low transformer profile for power dense packaging and improved thermal management. The HVS load voltage ripple was approximately 3 V with a 5-μF load capacitor. The load capacitor showed an RMS current of 6 A, while the voltage doubler capacitors showed RMS currents of 11 A. LVS lower-switch turn-on and turn-off currents of 78 A and 119 A, respectively, were obtained. Both LVS upper switches had zero current turn-on transitions, but had 108-A turn-off currents. However, the low duty cycle of these switches (4%) results in a switch RMS current value of 19 A (including the conduction of anti-parallel diode), as shown in table 2. Figure 6 shows the LVS upper and lower switch and inductor current waveforms. The clamp capacitor peak voltage was approximately 125 V. Based on its design features and favorable simulation results, the BCVD topology was selected for the converter implementation.

Table 2. Simulated component RMS current values (boost-mode, single-stage, 600-V, 5-kW load).

Component	Clamp Capacitor	Inductor	LVS Upper Switch	LVS Lower Switch	HVS Diode
RMS current (A)	26	99	19	130	15

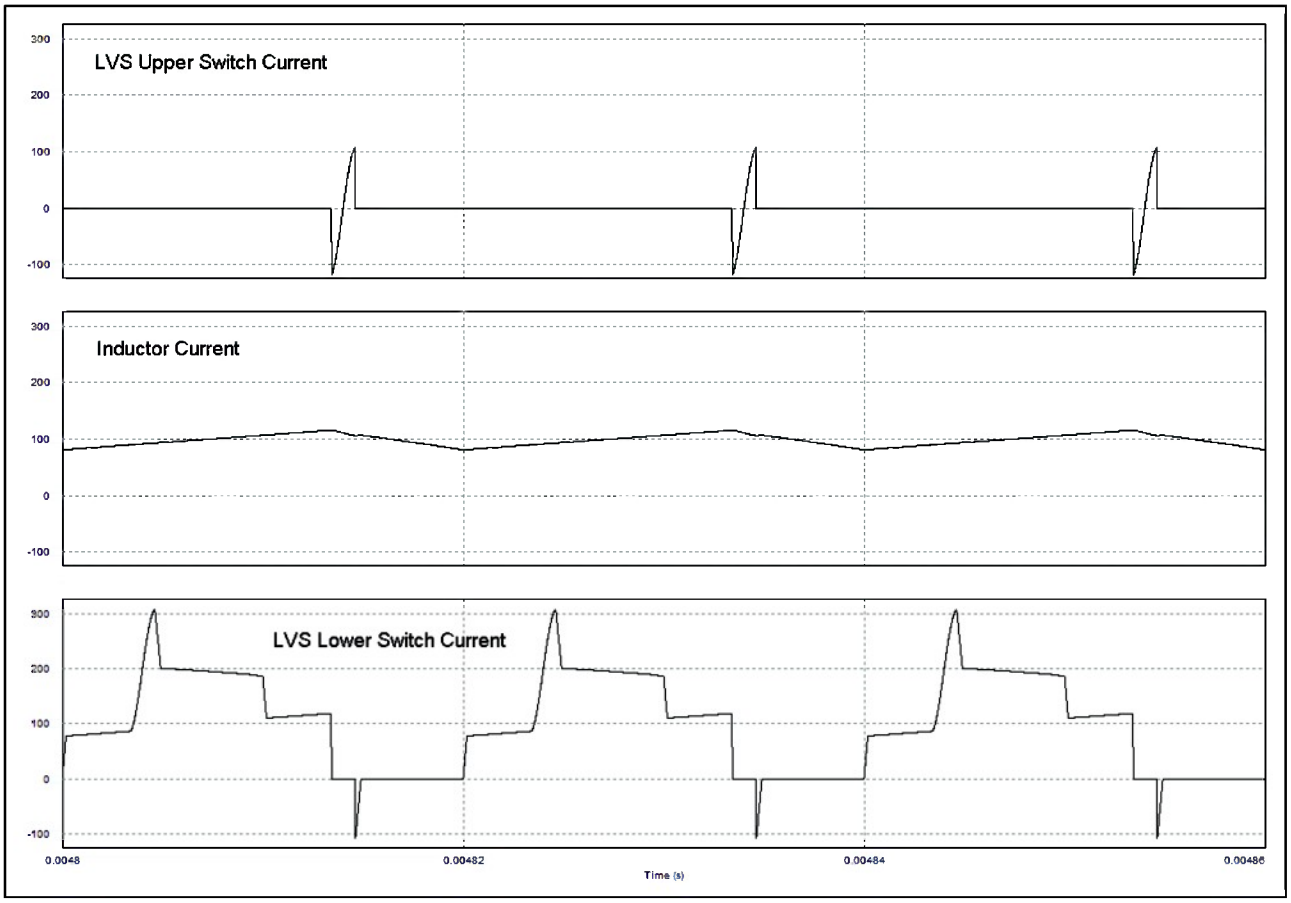

Figure 6. BCVD LVS: upper-switch, inductor, and lower-switch current waveforms (5-kW load).

4. Selection of Active Devices

4.1 LVS Switches

Following simulations, main converter components were identified for a TRL-4 converter test bed implementation. The use of commercial-off-the-shelf (COTS) components was preferred for initial converter development due to their availability, reliability, and low cost (compared to custom components). Components were selected, and de-rated to meet both the inlet coolant and ambient converter temperature specifications of 100 °C. Semiconductor devices have the greatest impact on the converter design based on available voltage rating, current ratings, and losses and were therefore selected first.

As mentioned previously, MOSFETs are favored for their low switching losses and their synchronous rectification capability. LVS devices were chosen first for their combination of high RMS currents and high switching frequency. Based on the simulated peak clamp capacitor voltage, MOSFETs with a 200-V drain-to-source breakdown voltage were selected for both the

upper and lower switches on the LVS. The LVS device configuration is compatible with common half-bridge switch modules, which typically have two symmetrically rated switches. The reduced inductance between the co-packaged switches in these modules is beneficial in power converters operating at high switching frequencies. However, in this application, the large difference in RMS current levels between the upper and lower switches, as shown in table 2, provides a volume, weight, and cost incentive to employ upper and lower switches having different current ratings.

Relationships of conduction loss versus current and switching energy versus current for the device candidates were used to estimate total device power loss. Thermal resistances of the switch modules and associated interface layers to the coolant were then used, along with loss data, to estimate device junction temperatures at a full load of 5 kW per converter stage. Semiconductor die temperatures were limited to 125 °C for the devices to provide a reliable operating margin below the 150 °C maximum rated junction temperature. The thermal resistances from COTS device packaging, the high coolant temperature, and the allowable device temperature rise of 25 °C resulted in a device RMS current de-rating of approximately 80% from the 25 °C datasheet rating. Switching loss and thermal calculations showed that for 100 °C coolant, less than one-fourth of the 80% RMS current de-rating was required for a switching frequency increase from 25 to 50 kHz. Although this tradeoff increases switch volume, a switching frequency of 50 kHz was selected reduce passive component volume by a factor of two.

One half-bridge MOSFET module and one single MOSFET module were selected to form each lower switch and its active clamp. With the half-bridge module having a lower current rating than the single module, the lower switch of the half-bridge module is connected in parallel with the single module to form a lower switch with a higher current rating. The remaining upper switch of the half-bridge module serves as the active clamp switch. Microsemi MOSFET modules APTM20AM04FG (half-bridge) and APTM20UM03FAG (single) were selected. The modules have 25 °C current ratings of 372 A and 580 A, respectively. An 80% de-rating results in values of 74 A and 116 A, respectively. By using two modules to form each half-bridge, the upper- and lower-switch ratings are 74 A and 190 A for 100 °C coolant. In both cases, these ratings exceed the simulated RMS upper- and lower-switch currents of table 2. In addition to having the same footprint (108 × 62 mm), which simplifies converter layout, the single switch module has drain and source terminal locations corresponding to those of the lower switch of the half-bridge module. This allows low inductance module interconnects to be made. Figure 7 shows a schematic of the module paring and physical models with terminal locations. The LVS design of each 5-kW converter stage includes four MOSFET modules.

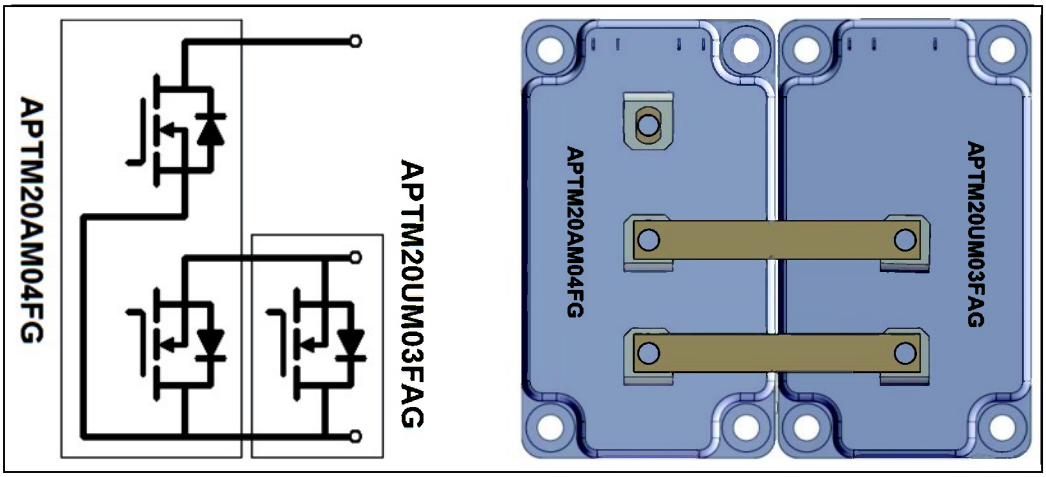

Figure 7. LVS module pairing schematic (left) and physical model (right).

4.2 HVS Switches

Insulated-gate bipolar transistor (IGBT) losses were compared to those of MOSFETs during the HVS device selection process. Although IGBTs and MOSFETs can be used interchangeably in many applications; synchronous rectification is not employed using IGBTs, but because it also provides significantly less efficiency gain on the HVS, it can be avoided in either device implementation. However, high IGBT switching losses requiring device de-ratings well in excess of 80%, prevented their use. The on-state resistances of MOSFETs in the 800- to 1000-V blocking range were found to be more than three times higher than those in the 400- to 500-V blocking range for comparable package size and switching energy loss at rated current. As a result, on-state current ratings for devices in the 800- to 1000-V blocking range were generally less than half of those in the 400- to 500-V blocking range. Therefore, changing the HVS configuration of each stage from a voltage doubler/half-bridge to a full-bridge configuration was considered to eliminate the need for paralleling more than two devices at each switch location. This change provides only half the HVS load voltage, and thus requires the HVS of both 5-kW converter stages to be placed in series instead of in parallel. Time interleaving of the two stages can still be used to reduce HVS load voltage ripple and/or HVS capacitor size.

Boost-mode converter simulations with the full-bridge HVS configuration, showed the same component RMS currents as shown in table 2 for the voltage doubler/half-bridge output stage. However, with the voltage doubling capacitors replaced by diodes, the RMS current of the same 5-µF load capacitance increased to 14 A. Load voltage ripple also increased to nearly 6 V with an RMS value of 3.6 V. Simulation of the 10-kW, two-stage interleaved converter resulted in a 2-V_{RMS} load voltage ripple at 200 kHz with a 5-µF capacitor on the HVS of each stage. A single MOSFET/diode module having a drain-to-source breakdown voltage of 500 V was selected for each switch of the full-bridge HVS stage. The MOSFET is a Microsemi APT50M38JLL in a SOT-227 (ISOTOP) package. The module has an 88-A rating at a junction temperature of 25 °C. De-rated 80% for operation with 100 °C coolant gives it an 18-A rating, which is greater

than the HVS diode RMS current from table 2. In total, the HVS design of each 5-kW converter stage includes four modules.

5. Buck-mode Simulations

The converter, with full-bridge HVS, was simulated in buck-mode to verify bidirectional operation, assess LVS operating range, and determine component electrical stresses. Synchronous rectification of the LVS was not modeled. Results showed sufficient duty cycle margin to produce full load voltage using only diode conduction on the LVS. Nominal load voltage was achieved with a duty cycle of 41%. Table 3 shows selected component RMS current values from a single-stage, buck-mode simulation. The same passive component values were used from the single-stage, boost-mode simulations at the same switching frequency of 50 kHz. A 0.15-Ω load (5 kW at 28 V) and a 1000-µF load capacitor were used. The large value of the LVS load capacitor was selected to reduce low side voltage and current ripple while preventing transient oscillations between the converter and battery pack from associated interconnect parasitic inductance. The LVS bulk capacitance can be implemented using high temperature aluminum electrolytic capacitors with relatively low component volume. The LVS load voltage ripple was less than 10 mV with a load capacitor RMS current of 3.4 A.

Table 3. Simulated component RMS current values (buck-mode, single-stage, 28 V, 5-kW load).

Component	Clamp Capacitor	Inductor	Load Capacitor	LVS Lower Diode	HVS Switch
RMS current (A)	0	90	3.4	121	15

6. Converter Voltage Characteristics

6.1 LVS and HVS Voltage Ranges

Following characterization at nominal source voltages under full single-stage loading, maximum and minimum source voltages in both buck- and boost-modes were used to assess converter input voltage ranges. The steady-state voltage ranges listed in table 1 are 25 to 29 V and 555 to 623 V for the LVS and HVS, respectively. The single-stage converter model was simulated in boost-mode at LVS voltages of 25 and 29 V, and in buck-mode at HVS voltages of 555 and 623 V to show that nominal load voltages could be met under all conditions. Table 4 shows the results of all four converter simulations, with the single-stage HVS voltage shown as half the two-stage converter load voltage. (This is due to the series HVS connection of the two 300-V HVS stages to form the 600-V HVS.) The buck-mode duty cycle is that of each set of complementary switches on the converter HVS. The boost-mode duty cycle corresponds to only the lower

switches on the LVS, with the upper switches of the LVS having a constant 4% duty cycle following a 2% dead-time interval. With the 2% dead-time interval between each set of upper and lower switches of the converter, maximum boost-mode and buck-mode duty cycles are 92% (lower switch) and 48%, respectively. The simulation results confirm that nominal converter load voltages can be met over the respective steady-state source voltage ranges in each mode of operation with sufficient duty cycle margins of 20.4% in boost-mode and 3.6% in buck-mode.

Table 4. Nominal load voltage simulation results at maximum and minimum supply voltages.

Mode	Supply Voltage (V)	Duty Cycle (%)	Load Voltage (V)
Buck	623/2	39.5%	28.0
	555/2	44.4%	28.0
Boost	29	65.7%	300.3
	25	71.6%	300.4

6.2 Distortion

The maximum distortion spectrums for both the 28- and 600-V vehicle busses are presented in the Stryker Modernization document (*1*). In each case, the maximum distortion spectrum provides the highest acceptable RMS amplitude of each harmonic component of the DC ripple voltage. For the design of this converter, the maximum distortion spectrums have been interpreted to apply to bus voltages to which power is sourced (i.e., the load voltages in buck and boost-modes). The maximum distortion spectrum for the LVS rises at 10 dBV per decade to a maximum amplitude of 0 dBV at 1 kHz and remains constant to 5 kHz. It then falls at 20 dBV per decade to a frequency of 50 kHz, and falls at 40 dB per decade thereafter. The LVS ripple voltage frequency for two synchronized stages of the selected converter topology is 100 kHz. For two interleaved stages the resultant ripple voltage frequency is 200 kHz. At each of these frequencies, the maximum RMS load voltage ripple allowances for the LVS are 2.50×10^{-2} V and 6.25×10^{-3} V, respectively.

The converter was simulated in buck-mode with two stages at a load power of 10 kW to determine LVS ripple. Table 5 shows the RMS ripple voltage amplitudes at the fundamental ripple frequency and higher frequency harmonics for a single LVS load capacitor (1000 μF), for both interleaved and synchronized switching between stages. Also included in table 5 are the maximum RMS ripple voltage amplitudes defined by the 28-V DC bus maximum distortion spectrum. The simulation results presented in table 5 show that the distortion spectrum can be met using either interleaved or synchronized operation of the two-stage converter in buck-mode.

Table 5. Buck-mode RMS load ripple voltage allowance vs. simulated two-stage converter results.

Ripple Frequency Component RMS (V)					
	100 kHz	200 kHz	300 kHz	400 kHz	500 kHz
Distortion allowance	2.50×10^{-2}	6.25×10^{-3}	2.78×10^{-3}	1.56×10^{-3}	1.00×10^{-3}
Two-stage interleaved	2.54×10^{-4}	1.97×10^{-3}	1.04×10^{-7}	1.59×10^{-4}	1.03×10^{-5}
Two-stage synchronized	9.76×10^{-3}	1.97×10^{-3}	5.93×10^{-4}	1.59×10^{-4}	4.57×10^{-6}

The maximum distortion spectrum for the HVS has a nearly identical trend as that of the LVS. However, the vertical scale is represented in units of dBμV. In boost-mode, the fundamental load voltage ripple frequency for a single stage or for two stages without interleaving (synchronized) is 100 kHz. For two interleaved stages, it is 200 kHz. At each of these frequencies, the maximum RMS load voltage ripples for the HVS are 1.41×10^{-1} V and 3.51×10^{-2} V, respectively. Simulation of the two-stage synchronized boost-mode converter model showed an RMS ripple voltage amplitude of 6.77 V. Although this value corresponds to just over 1% RMS ripple, it greatly exceeds the specification at 100 kHz. Even, the simulation result for the two-stage interleaved boost-mode converter model showed an RMS ripple voltage amplitude of 1.87 V—far exceeding the specification at 200 kHz. The simulations were conducted using the 5-μF HVS capacitor value for each stage from previous simulations. To meet the RMS ripple voltage specification at each HVS fundamental frequency, load capacitor values exceeding 230 and 370 μF per stage, are required for synchronized and interleaved operation, respectively. These results show that the HVS ripple specification can be met using a smaller capacitor without interleaving.

7. Passive Component Selection

To achieve a high converter power density while meeting the high operating temperature specification, passive components having these same attributes were selected. Based on the 28-V LVS bus, low impedance, high temperature (125 °C) aluminum electrolytic capacitors were chosen. Capacitance values are 1000 μF per component, with an equivalent series resistance (ESR) of 34 mΩ. To distribute the capacitance at the converter LVS bus, provide increased RMS current margin, and further reduce equivalent ESR and equivalent series inductance (ESL), all without substantially impacting converter volume, ten capacitors (Nippon Chemicon, EGPA500EXX102MK35S) were selected to be placed in parallel. Next, the active clamp capacitors require an ultra-low ESR/ESL capacitor type for high transient current operation. To meet this requirement, a very limited selection of high temperature film capacitors are available. Polycarbonate/foil semi-custom film capacitors rated at 0.27 μF and 1 kV for operation at 125 °C were selected (Electronic Concepts, CT2-12283K). Four capacitors were placed in parallel for each 1-μF active clamp capacitor for less than 7 A_{RMS} per part. Finally, the series connected capacitors at the HVS of each converter stage were selected to have a rating of 500 V. Due to

the high capacitance value needed to meet the HVS ripple specification, the high voltage rating, the high temperature requirement, and relatively low RMS current, six 39-µF stacked ceramic chip capacitor arrays (AVX, SM067C396KHJ650) were chosen for each converter stage. A smaller 5.6-µF capacitor (AVX, SM037C565KHJ650) was added for each converter stage to meet the HVS ripple voltage specification under nominal capacitance values. Input capacitances of HVS system loads could reduce the required HVS capacitance. Table 6 lists the power-stage components for the total two-stage converter design.

Table 6. Main power components for the two-stage BCVD converter.

Part Description	Part No.	Manufacturer	Quantity
200-V half-bridge MOS module LVS	APTM20AM04FG	Microsemi	4
200-V single MOS module LVS	APTM20UM03FAG	Microsemi	4
500-V single MOS module HVS	APT50M38JLL	Microsemi	8
50-V, 1000-µF LVS capacitor	EGPA500EXX102MK35S	Nippon Chemicon	10
1000-V, 0.27-µF clamp capacitor	CT2-12283K	Electronic Concepts	8
500-V, 39-µF HVS capacitor	SM067C396KHJ650	AVX	12
500-V, 5.6-µF HVS capacitor	SM037C565KHJ650	AVX	2
10 µH, 50 kHz ferrite planar inductor	PQC1406	Planar Quality Corp.	4
2:8, 50 kHz ferrite planar transformer	PQC1446	Planar Quality Corp.	2

Planar inductors and transformers were chosen for their thermal management and low leakage inductance advantages previously mentioned. Custom inductors (Planar Quality Corporation, PQC1406) having a value of 10 µH and approximate dimensions of 145 mm × 87 mm × 28 mm were custom designed for this application. Transformers (Planar Quality Corporation PQC1446) having a turns ratio of 2:8 and approximate dimensions of 145 mm × 76 mm × 35 mm were also custom designed. Both parts made use of COTS ferrite cores. Each converter stage would require two inductors and one transformer. Both parts were rated for continuous operation at their respective simulated maximum continuous RMS currents for a heat sink and ambient temperature of 100 °C.

8. TRL-4 Converter Packaging

A preliminary packaging design was made for the COTS components of the bidirectional converter for high power density. In addition to power components, high temperature gate drive and controller hardware was included from estimated layout modifications to existing high temperature circuits. A custom aluminum heat sink based the Lytron CP30 cold plate, having a thermal resistance of 0.189 °C/W, was used in the design. Chomerics Thermflow T777 phase change thermal interface material was modeled as the interface between the heat sink and the switch modules and magnetic components. Parts were positioned on only the top side of the heat sink to keep circuit inductances low. Figure 8 shows a computer-aided drafting (CAD) image of

the package design with an outer envelope representing the converter enclosure (74 cm × 33 cm × 8 cm).

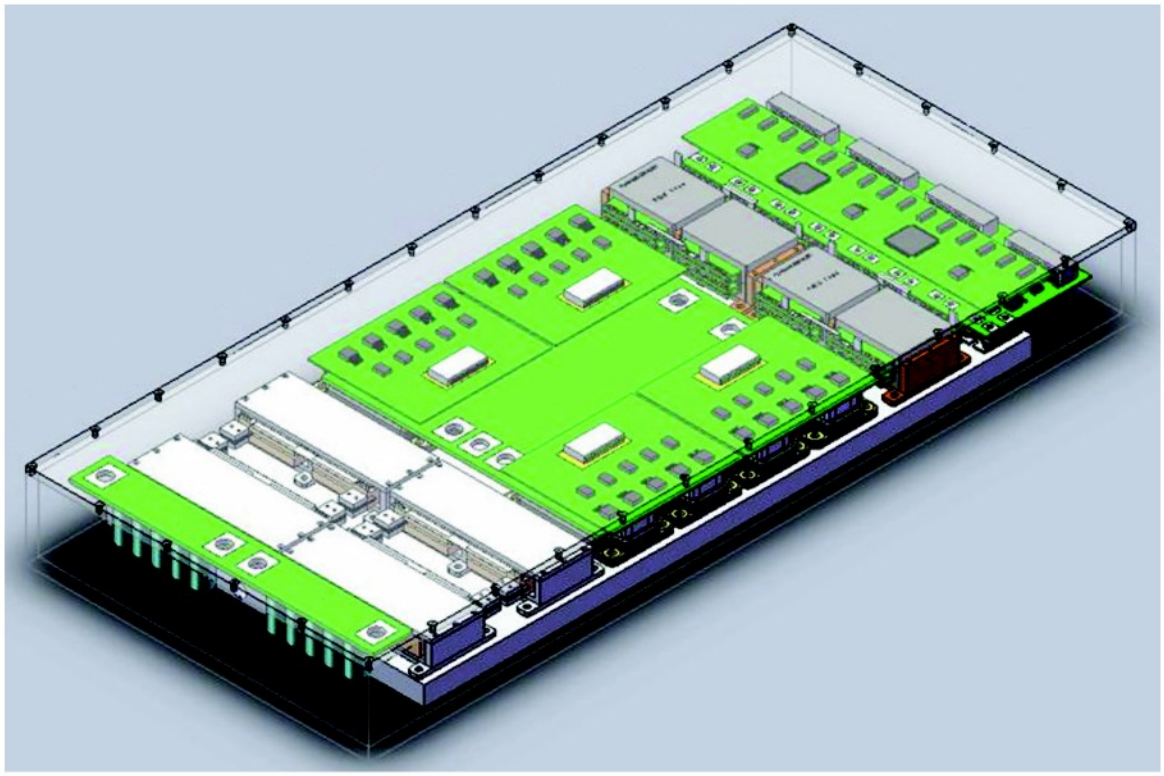

Figure 8. CAD image of bidirectional converter package design.

Figure 9 shows a breakdown of the converter design with a circuit board cutaway exposing components on the bottom half of the image. Nearly all of the board-to-component and board-to-board connections are made by direct board-to-terminal or plug connections. Plumbing connections, power cable connections, wire harnesses, and sensors are not shown in the package model, but can be included in open areas on the input side of the converter (left side) and in the center of the converter. These components were considered in the converter envelope. Figure 10 presents converter volume estimates for three switching frequencies considered. Additionally, for each switching frequency, percent volume estimates of converter components are shown. Both the 25- and 100-kHz switching frequencies show larger total component volumes than that at 50 kHz.

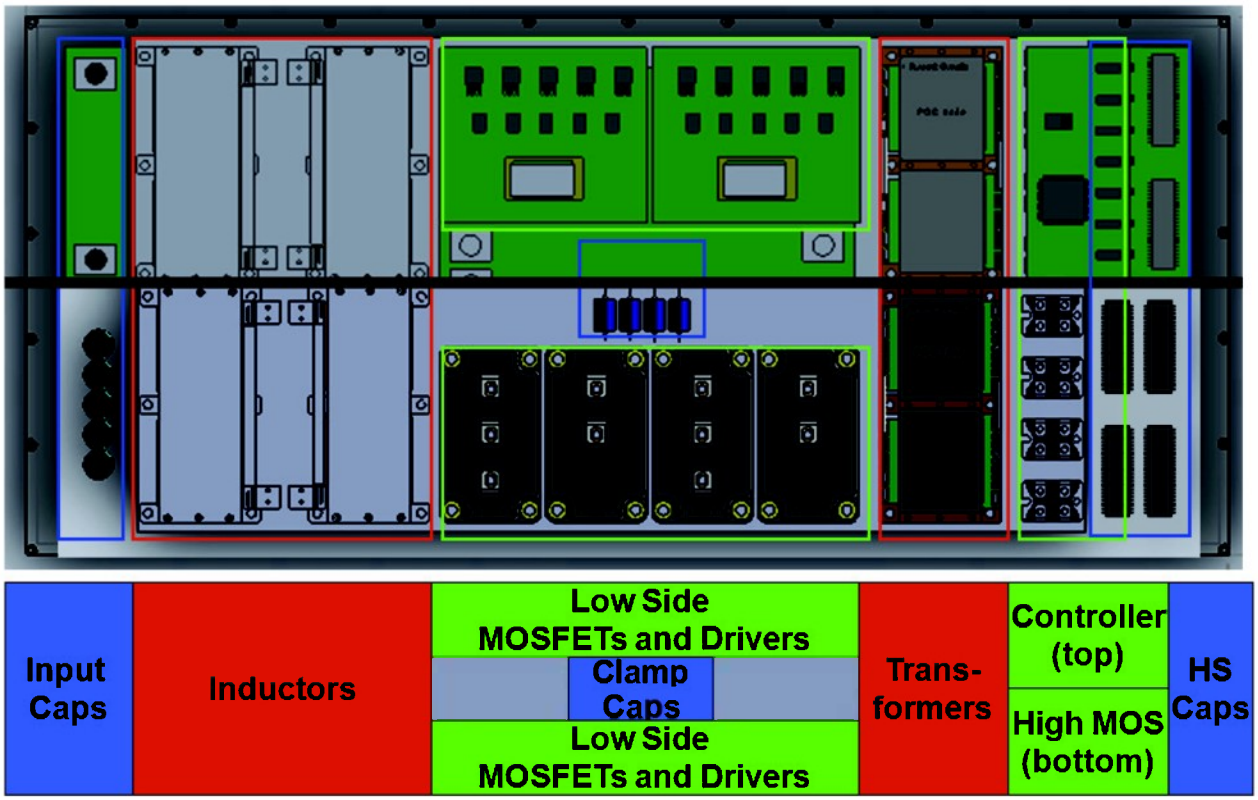

Figure 9. Converter cutaway showing components and layers.

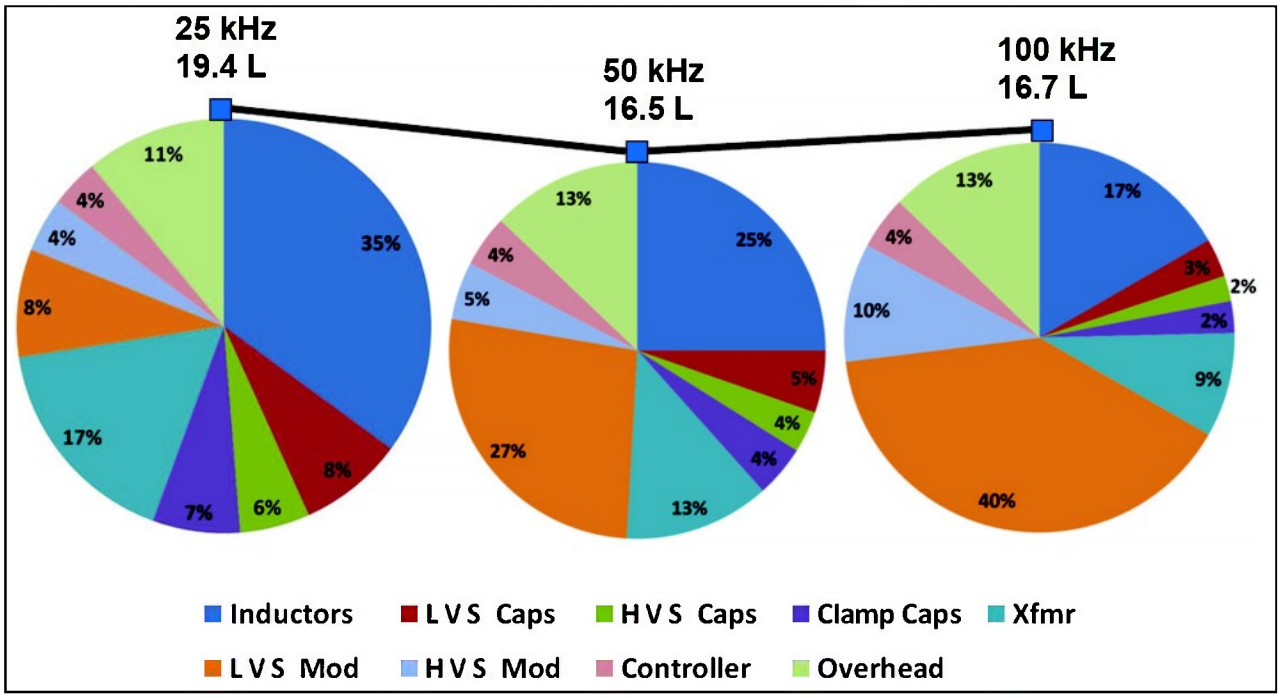

Figure 10. Estimated converter volumes and component volume percentages vs. switching frequency.

9. Thermal Performance and Silicon-carbide Insertion

The circuit simulation and datasheet driven MOSFET modeling used to estimate losses and junction temperatures during the device selection process was used to compare the COTS silicon (Si) devices to SiC devices. SiC device data was obtained from converter application testing of 1200-V, 50-A (nominal), 0.56-cm^2 MOSFETs and 1200-V, 50-A (nominal), 0.31-cm^2 junction barrier Schottky (JBS) diodes (*3*). Two options for Si replacement using SiC devices were considered. One option is the replacement of HVS devices only (Option 1), and the other is a replacement of both LVS and HVS Si components (Option 2). Simulations were run for operation using diode rectification, as a basis from which further efficiency improvements can be made in all cases using synchronous rectification.

Options 1 and 2 consider SiC devices in the same COTS module packages selected for the Si implementation. Simulations showed that seven SiC MOSFET/JBS diode pairs were required to meet each LVS lower-switch and diode-current requirement. Although the LVS upper-switch and diode-current requirements are significantly lower, a dual module with symmetric lower- and upper-switch/diode current ratings was considered for its applicability to other converter topologies. Simulations also showed that one SiC MOSFET/JBS diode pair would meet the HVS module current requirements. The LVS module package can be populated with seven 0.56-cm^2 SiC MOSFETs and seven 0.31-cm^2 JBS diodes for each of the upper- and lower-switch/diode pairs, as evidenced by previous U.S. Army Research Laboratory (ARL) work (*4*). The HVS SOT-227 module package can accommodate one such SiC MOSFET and JBS diode pair. The simulations allowed for the higher SiC device junction temperature of approximately 150 °C using the same package thermal resistances. The proposed SiC implementation on the LVS requires half the number of modules as the Si design. The higher blocking voltage capability of the SiC devices also allows the HVS configuration to be changed back to the original half-bridge/voltage doubler design, thereby requiring half the number of high side devices compared to the Si approach. However, the simulation results show a tradeoff between the related power density and thermal advantages versus converter efficiency for SiC on the LVS. Tables 7 and 8 show simulation results of switch/diode power losses and maximum device junction temperatures for the COTS Si implementation and SiC Options 1 and 2 for boost- and buck-modes, respectively.

Table 7. Boost-mode simulated switch/diode power losses and maximum device junction temperatures.

Boost-Mode	COTS Silicon	Option 1	Option 2
LVS	144 W, 592 W	144 W, 592 W	280 W, 840 W
MOS: Upper, Lower	110 °C, 116 °C	110 °C, 116 °C	109 °C, 128 °C
HVS	264 W	68 W	68 W
Diode	122 °C	136 °C	136 °C

Table 8. Buck-mode simulated switch/diode power losses and maximum device junction temperatures.

Buck-Mode	COTS Silicon	Option 1	Option 2
LVS	300 W	300 W	696 W
Diode	111 °C	111 °C	152 °C
HVS	328 W	196 W	196 W
MOS	121 °C	145 °C	145 °C

The results show that while Option 1 improves HVS efficiency, Option 2 reduces LVS efficiency as well as overall converter efficiency. Although conduction losses are nearly 25% higher for the SiC LVS lower switch, the majority of the increased loss on the LVS is attributed to switching losses. Option 1 is recommended for increasing converter efficiency and reducing the number of devices, and is therefore considered to be a valued investment in SiC technology. Synchronous rectification using SiC MOSFETs has been evaluated in a buck converter and has been shown to reduce losses by up to 50% (*5*). Although synchronous rectification was not simulated for this study, based on previous results, similar efficiency gains could be realized for both Si and SiC devices for this topology. In that case the loss savings using COTS Si should be smaller than those shown in tables 7 and 8. However, for synchronous rectification operation, it is not clear that Option 2 represents a viable SiC investment, even though this option halves the number of required LVS switch modules, increasing converter power density.

10. Conclusion

This report has presented the design of a 10-kW, bidirectional, 28- to 600-V, high temperature, converter power-stage in support of the GCS heavy brigade combat vehicle modernization program. Design considerations for five potential converter topologies were analyzed, simulated, and compared. A bidirectional, current-fed, converter with a LVS active clamp and configurable voltage doubling HVS was selected for its ability to meet the high voltage conversion ratio, and high power density requirements, while operating at a 50-kHz switching frequency. Bidirectional converter simulations of both single-stage and two-stage synchronized and interleaved operation were performed to assess operating margins over source voltage ranges and to identify component values to meet distortion spectrum specifications. It was determined that synchronized operation of the two-stage converter, resulting in a ripple frequency of 100 kHz, required a lower HVS load capacitance to meet the HVS distortion spectrum. The large LVS load capacitance also allowed the buck-mode distortion spectrum to be met for the same ripple frequency. This allowed simplified control compared to an interleaved approach.

Converter design and component selection allow for synchronous rectification to reduce system losses. However, the power-stage was designed to be able to operate with sufficient thermal margin without synchronous rectification. Both active and passive devices were specified for a

low-risk COTS implementation and analyses of component volume reductions and loss savings for two SiC device replacement options was shown. The option to replace only the HVS converter devices with 1200-V SiC MOSFETs with anti-parallel 1200-V SiC JBS diodes was recommended to provide a significant loss reduction while minimizing cost and risk. A power-dense, three-dimensional model of the proposed converter package design, including sensor and control hardware, was presented along with a comparison of component size contributions versus converter switching frequency supporting the selected 50-kHz operating point.

The design presented for the converter power-stage is supported by a digital control architecture developed for existing high temperature TRL-4 converters and test beds. The gate drives, sensors, and control hardware platform are flexible in their application to a wide range of pulse width modulated converters and can be scaled or optimized for each implementation. Although a detailed risk analysis of the converter design was not performed, the selected components and design provide sufficient operating margins for a COTS high temperature implementation. Additionally, the assumptions made and results shown in this hardware investigation may not apply to other designs.

11. References

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List of Symbols, Abbreviations, and Acronyms

ARL	U.S. Army Research Laboratory
BCVD	bidirectional, current-fed, voltage doubling
CAD	computer-aided drafting
COTS	commercial-off-the-shelf
ESL	equivalent series inductance
ESR	equivalent series resistance
GCS	Ground Combat Systems
HVS	high-voltage-side
JBS	junction barrier Schottky
IGBT	insulated-gate bipolar transistor
LVS	low-voltage-side
MOSFETs	metal oxide semiconductor field effect transistors
RMS	root mean square
Si	silicon
SiC	silicon carbide
TRL	technical readiness level
ZCS	zero current switching

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